REMARKS

The office action of April 5, 2005, has been reviewed and its contents carefully noted. Reconsideration of this case, as amended, is requested. Claims 1 through 28 remain in this case.

Preliminary Comments

The numbered paragraphs below correspond to the numbered paragraphs in the Office Action.

Rejection(s) under 35 U.S.C. §103

1-8) Claims 1-6, 8-14, 16, 17, 19, 22, 23 and 28 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Farnworth et al. in view of Hitachi Chemical Co. ("Epoxy Molding Compounds", 2003) and Pace.* Applicants respectfully traverse.

The present invention comprises a module where a solid state device is located between and bonded to two pieces of ceramic material, a strip line bonded to the two pieces of ceramic, one of the ceramic materials having terminals for conducting electrical signals, and the entire module being encapsulated by an epoxy having a similar coefficient of thermal expansion (CTE) as both the ceramic material and the strip line.

Farnworth et al. disclose packaged solid state assemblies, specifically "stacked" assemblies. However, they do not refer to a strip line. In contrast, Applicants claim that their solid state device does include a strip line (please note page 6, lines 6-11, of Applicants' specification for a description thereof).

The term "strip line" (also called "microstrip line") is well known in the art (please note pages 10-17 of the 2002 publication of Directed Energy, Inc. of Fort Collins, Colorado, entitled "Operation Manual" for a Laser Diode Driver, as well as pages 29-23 to 29-25 of "Reference Data for Engineers", Howard Sams & Co., 7th Ed.1989, copies of which is herewith provided for the convenience of the Examiner). Specifically, a strip line must have a pulse and a return (or strip and ground plane) on opposite sides of an insulated strip (kindly note the first full paragraph on page 10, and Figures 3 and 4, of the Directed Energy publication, or fig. 22 on page 29-23 of

"Reference Data"). Thus, the current on one conductor flows in the opposite direction from the current on the other conductor. This causes the inductance of the strip to be very low, which is important in pulse power applications.

The elements identified by Examiner as a "strip line" (36), (36) and (50) are not a strip line - they are two separate lines leading to the device and an unrelated insulator. These do not make a "stripline", as that term is known to the art and used in the present application.

If Farnworth et al. had intended to describe a strip line in their disclosure, then why did they not use this term? Applicants respectfully submit that the reason is because their concept does not contemplate devices that comprise strip lines, as defined and claimed in the instant patent application.

Further, the reference does not show two ceramic substrates bonded to a solid state device. The first ceramic substrate (12) is bonded to a semiconductor, but the other such substrate (12A), as shown in Figure 2D, lies above the first ceramic substrate, thus creating a "stacked" semiconductor die configuration. This second ceramic substrate is not bonded to the semiconductor, as Applicants claim.

Pace discloses a packaging module for bonding semiconductor power devices. The focus of this patent is the thermal conductivity of the pads separating the power devices and a substrate. Specifically, Pace utilizes a frame that is bonded to both the semiconductor power device and the substrate between which it lies. Metal protuberances are used to make the electrical connections. In contrast, the present invention does not claim the use of a framing structure nor metal protuberances for electrical conductivity.

The Hitachi reference describes epoxies having CTE's similar to silicon. However, Applicants are not trying to claim the uniqueness of this correlation. What Applicants are claiming is the use of epoxies having CTE's similar to silicon within the context of many other features a packaged solid state device. Reconsideration and withdrawal of the rejection are respectfully requested.

9-10) Regarding the rejection of independent claim 17, Applicants respectfully submit that since it is their contention that the assembly defined in claim 1 is patentable over the cited

references, as discussed hereinabove, then the method of this claim, et seq., is also patentable. Farnworth et al. do not disclose or even suggest that Applicants' claimed method of packaging a solid state device that includes a strip line, in addition to other elements and features. Reconsideration and withdrawal of the rejection are respectfully requested.

13) *[sic]* Claims 7, 15 and 27 are rejected under 35 USC 103(a) as being unpatentable over Farnworth et al., as applied to Claims 1-6, 8-14, 16, 17, 19, 22, 23 and 28 and further in view of Nagesh et al. As noted by the Examiner, Nagesh et al. disclose a heat sink in contact with a substrate, the latter comprising, among other materials, ceramic. However, these heat sinks are disclosed as being used with multi-chip electronic modules. There is nothing in the disclosure or teaching of this reference that refers to strip lines. It is respectfully submitted that the combined teachings of both Farnworth et al. and Nagesh et al. fail to render obvious Applicants' claimed subject matter. Reconsideration and withdrawal of the rejection are respectfully requested.

16-17) Claims 18, 20 and 21 are rejected under 35 USC 103(a) as being unpatentable over Farnworth et al., as applied to Claims 1-6, 8-14, 16, 17, 22, 23 and 28 and further in view of Chen et al. Applicants respectfully submit that, in view of the foregoing arguments in support of the patentability of claims 1 et seq. and 17 et seq., the further citation of Chen et al. fails to render obvious the subject matter of these dependent claims. Reconsideration and withdrawal of the rejection are respectfully requested.

18-19). Claim 24 is rejected under 35 USC 103(a) as being unpatentable over Farnworth et al., as applied to Claims 1-6, 8-14, 16, 17, 19, 22, 23 and 28 and further in view of Kazama et al. Applicants respectfully submit that the addition of the teaching of Kazama et al. to Farnworth et al. would not have lead one in the art to the use of a reflow oven to solder the terminals of the solid state assembly as defined in claim 17. Reconsideration and withdrawal of the rejection are respectfully requested.

20-21) Claim 26 is rejected under 35 USC 103(a) as being unpatentable over Farnworth et al., in view of Kazama et al., as applied to Claims 1-6, 8-14, 16, 17, 19, 22, 23 and 28 and further in view of Nguyen. Applicants respectfully submit that the additional citation of Nguyen fails to render obvious the claimed subject matter in view of the arguments previously presented

with respect to Farnworth et al. and Kazama et al. Reconsideration and withdrawal of the rejection are respectfully requested.

Conclusion

Applicant believes the claims, as filed, are patentable over the prior art, and that this case is now in condition for allowance of all claims therein. Such action is thus respectfully requested. If the Examiner disagrees, or believes for any other reason that direct contact with Applicants' attorney would advance the prosecution of the case to finality, he is invited to telephone the undersigned at the number given below.

"Recognizing that Internet communications are not secured, I hereby authorize the PTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file."

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